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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/628,443	07/29/2003	Hiroaki Doi	056203.52639US	5303

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EXAMINER	
WILLIAMS, ALEXANDER O	
ART UNIT	PAPER NUMBER
2826	

DATE MAILED: 07/01/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/628,443	DOI ET AL.	
	Examiner	Art Unit	
	Alexander O. Williams	2826	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *07 April 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Serial Number: 10/628443 Attorney's Docket #: 056203.52639US
Filing Date: 7/29/2003; claimed foreign priority to 2/18/2003

Applicant: Doi et al.

Examiner: Alexander Williams

Applicant's Amendment filed 4/7/05 to the election of species of figures 1-6 (claims 1 to 20), filed 10/18/04, has been acknowledged.

The following is a quotation of the appropriate paragraphs of 35 U.S.C. § 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(f) or (g) prior art under 35 U.S.C. 103(a).

Claims 1 to 4 and 9 to 20 are rejected under 35 U.S.C. § 102(b) as being anticipated by Tsuji et al. (European Patent Application Publication # 0484180 A1).

1. Tsuji et al. (figures 2A to 10B) specifically figure 2A show an electronic circuit device comprising, an electronic circuit element **1**, a substrate **2** including a front surface on which the electronic circuit element is mounted and a reverse surface opposite to the front surface in a thickness direction of the substrate, an electrically conductive terminal member **3** electrically connected to the electronic circuit element, a lead frame **10** extending perpendicular to the thickness direction to face the reverse surface in the thickness direction, and a sealing resin **5** covering at least partially the electronic circuit element, substrate and lead frame while at least a part of the electrically conductive terminal member is prevented from being covered by the sealing resin **(outer portion of 3 outside of 5 of the device)**, wherein in a cross sectional view taken along an imaginary plane passing the substrate and lead frame and extending parallel to the thickness direction, the substrate extends to project outward with respect to an end of the lead frame in a transverse direction perpendicular to the thickness direction while the end of the lead frame is covered by the sealing resin.
2. An electronic circuit device according to claim 1, Tsuji et al. show wherein a coefficient of linear expansion of the lead frame in the transverse direction is smaller than a coefficient of linear expansion of the sealing resin (inherit since Applicant's material for the lead frame and sealing resin is the same as the prior art).
3. An electronic circuit device according to claim 1, Tsuji et al. show wherein a difference in coefficient of linear expansion in the transverse direction between the substrate and the lead frame is smaller than a difference in coefficient of linear expansion in the transverse direction between the sealing resin and the lead frame.
4. An electronic circuit device according to claim 1, Tsuji et al. further comprising a resin adhesive **(inherit)** through which the lead frame is adhered to the reverse surface (inherit since Applicant's material for the lead frame and sealing resin is the same as the prior art).
9. An electronic circuit device according to claim 1, Tsuji et al. show wherein the imaginary plane extends parallel to a longitudinal direction of the at least a part of the electrically conductive terminal member.
10. An electronic circuit device according to claim 1, Tsuji et al. show wherein the electronic circuit device comprises a plurality of the electrically conductive terminal members **3** juxtaposed in an electrically conductive terminal member array direction, and the imaginary plane extends perpendicular to the electrically conductive terminal member array direction.

11. An electronic circuit device according to claim 1, Tsuji et al. show wherein the lead frame is formed in one-piece, a part of the lead frame in one-piece is prevented from being covered by the sealing resin to protrude from the sealing resin in a protruding direction perpendicular to the thickness and transverse directions, and the imaginary plane extends perpendicular to the protruding direction.

12. An electronic circuit device according to claim 11, Tsuji et al. show wherein the lead frame has a surface facing to the reverse surface in the thickness direction and prevented from being covered by the sealing resin to protrude from the sealing resin in the protruding direction.

13. An electronic: circuit device according to claim 1, Tsuji et al. show wherein in the cross sectional view, the substrate extends to project outward in the transverse direction with respect to another end of the lead frame opposite to the end of the lead frame in the transverse direction while the another end of the lead frame is covered by the sealing resin.

14. An electronic circuit device according to claim 13, Tsuji et al. show wherein a part of the lead frame is prevented from being covered by the sealing resin to protrude from the sealing resin in a protruding direction perpendicular to the thickness and transverse directions, and a width between the another end and the end in the cross sectional view is smaller than a width of the part of the lead frame in the transverse direction.

15. An electronic circuit device according to claim 13, Tsuji et al. show wherein in the cross sectional view, a width of the lead frame between the another end and the end is not more than 80 % of a width of the substrate.

16. An electronic circuit device according to claim 1, Tsuji et al. show wherein the electronic circuit element includes a semiconductor body whose main component is a semiconductor, and as seen in the thickness direction, the semiconductor body and the lead frame overlap with each other.

17. An electronic circuit device according to claim 16, Tsuji et al. show wherein the electronic circuit element includes a power transistor.

18. An electronic circuit device according to claim 16, Tsuji et al. show wherein as seen in the thickness direction, the whole of the semiconductor body overlaps with the lead frame.

19. An electronic circuit device according to claim 1, Tsuji et al. show wherein the lead frame is prevented from being electrically connected to the electronic circuit element.

20. An electronic circuit device according to claim 1, Tsuji et al. show wherein the lead frame is metallic, and a main component of the substrate is a ceramic.

Claims 1 to 4 and 9 to 20 are rejected under 35 U.S.C. § 102(b) as being anticipated by (Japan Patent Application Publication # 5-82573).

1. (Japan Patent Application Publication # 5-82573) (figures 1 to 5) specifically figure 5 show an electronic circuit device comprising, an electronic circuit element **6**, a substrate **9** including a front surface on which the electronic circuit element is mounted and a reverse surface opposite to the front surface in a thickness direction of the substrate, an electrically conductive terminal member **11** electrically connected to the electronic circuit element, a lead frame **13** extending perpendicular to the thickness direction to face the reverse surface in the thickness direction, and a sealing resin **14** covering at least partially the electronic circuit element, substrate and lead frame while at least a part of the electrically conductive terminal member is prevented from being covered by the sealing resin **(outer portion of 11 outside of 14 of the device)**, wherein in a cross sectional view taken along an imaginary plane passing the substrate and lead frame and extending parallel to the thickness direction, the substrate extends to project outward with respect to an end of the lead frame in a transverse direction perpendicular to the thickness direction while the end of the lead frame is covered by the sealing resin.
2. An electronic circuit device according to claim 1, (Japan Patent Application Publication # 5-82573) show wherein a coefficient of linear expansion of the lead frame in the transverse direction is smaller than a coefficient of linear expansion of the sealing resin (inherit since Applicant's material for the lead frame and sealing resin is the same as the prior art).
3. An electronic circuit device according to claim 1, (Japan Patent Application Publication # 5-82573) show wherein a difference in coefficient of linear expansion in the transverse direction between the substrate and the lead frame is smaller than a difference in coefficient of linear expansion in the transverse direction between the sealing resin and the lead frame.
4. An electronic circuit device according to claim 1, (Japan Patent Application Publication # 5-82573) further comprising a resin adhesive **10** through which the lead frame is adhered to the reverse surface (inherit since Applicant's material for the lead frame and sealing resin is the same as the prior art).

9. An electronic circuit device according to claim 1, (Japan Patent Application Publication # 5-82573) show wherein the imaginary plane extends parallel to a longitudinal direction of the at least a part of the electrically conductive terminal member.
10. An electronic circuit device according to claim 1, (Japan Patent Application Publication # 5-82573) show wherein the electronic circuit device comprises a plurality of the electrically conductive terminal members **11** juxtaposed in an electrically conductive terminal member array direction, and the imaginary plane extends perpendicular to the electrically conductive terminal member array direction.
11. An electronic circuit device according to claim 1, (Japan Patent Application Publication # 5-82573) show wherein the lead frame is formed in one-piece, a part of the lead frame in one-piece is prevented from being covered by the sealing resin to protrude from the sealing resin in a protruding direction perpendicular to the thickness and transverse directions, and the imaginary plane extends perpendicular to the protruding direction.
12. An electronic circuit device according to claim 11, (Japan Patent Application Publication # 5-82573) show wherein the lead frame has a surface facing to the reverse surface in the thickness direction and prevented from being covered by the sealing resin to protrude from the sealing resin in the protruding direction.
13. An electronic: circuit device according to claim 1, (Japan Patent Application Publication # 5-82573) show wherein in the cross sectional view, the substrate extends to project outward in the transverse direction with respect to another end of the lead frame opposite to the end of the lead frame in the transverse direction while the another end of the lead frame is covered by the sealing resin.
14. An electronic circuit device according to claim 13, (Japan Patent Application Publication # 5-82573) show wherein a part of the lead frame is prevented from being covered by the sealing resin to protrude from the sealing resin in a protruding direction perpendicular to the thickness and transverse directions, and a width between the another end and the end in the cross sectional view is smaller than a width of the part of the lead frame in the transverse direction.
15. An electronic circuit device according to claim 13, (Japan Patent Application Publication # 5-82573) show wherein in the cross sectional view, a width of the lead frame between the another end and the end is not more than 80 % of a width of the substrate.

16. An electronic circuit device according to claim 1, show wherein the electronic circuit element includes a semiconductor body whose main component is a semiconductor, and as seen in the thickness direction, the semiconductor body and the lead frame overlap with each other.
17. An electronic circuit device according to claim 16, (Japan Patent Application Publication # 5-82573) show wherein the electronic circuit element includes a power transistor.
18. An electronic circuit device according to claim 16, (Japan Patent Application Publication # 5-82573) show wherein as seen in the thickness direction, the whole of the semiconductor body overlaps with the lead frame.
19. An electronic circuit device according to claim 1, (Japan Patent Application Publication # 5-82573) show wherein the lead frame is prevented from being electrically connected to the electronic circuit element.
20. An electronic circuit device according to claim 1, (Japan Patent Application Publication # 5-82573) show wherein the lead frame is metallic, and a main component of the substrate is a ceramic.

Initially, and with respect to claims 5-8, note that a "product by process" claim is directed to the product per se, no matter how actually made, In re Hirao, 190 USPQ 15 at 17 (footnote 3). See also In re Brown, 173 USPQ 685; In re Luck, 177 USPQ 523; In re Wertheim, 191 USPQ 90 (209 USPQ 554 does not deal with this issue); In re Fitzgerald, 205 USPQ 594, 596 (CCPA); In re Marosi et al., 218 USPQ 289 (CAFC); and most recently, In re Thorpe et al., 227 USPQ 964 (CAFC, 1985) all of which make it clear that it is the final product per se which must be determined in a "product by process" claim, and not the patentability of the process, and that, as here, an old or obvious product produced by a new method is not patentable as a product, whether claimed in "product by process" claims or not. Note that Applicant has burden of proof in such cases as the above case law makes clear.

Claims 5-8 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Tsuji et al. (European Patent Application Publication # 0484180 A1).

The examiner is only interested in finding the claimed final structure I the claimed invention.

As to the grounds of rejection under section 103, see MPEP § 2113.

Claims 5-8 are rejected under 35 U.S.C. § 103(a) as being unpatentable over (Japan Patent Application Publication # 5-82573).

The examiner is only interested in finding the claimed final structure I the claimed invention.

As to the grounds of rejection under section 103, see MPEP § 2113.

Response

Applicant's arguments filed 4/7/05 have been fully considered, but are moot in view of the new grounds of rejections detailed above.

The listed references are cited as of interest to this application, but not applied at this time.

Field of Search	Date
U.S. Class and subclass: 257/787,676,783,666,685,686,777,702,703,705,773,723, 528,533,712,713,717,720,675,724,725,728 361/705,719,704,748	1/9/05 6/23/05
Other Documentation: foreign patents and literature in 257/787,676,783,666,685,686,777,702,703,705,773,723, 528,533,712,713,717,720,675,724,725,728 361/705,719,704,748	1/9/05 6/23/05
Electronic data base(s): U.S. Patents	1/9/05 6/23/05

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Alexander O Williams whose telephone number is (571) 272 1924. The examiner can normally be reached on M-F 6:30-7:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan Flynn can be reached on (571) 272 1915. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Alexander O Williams
Primary Examiner
Art Unit 2826

AOW
6/23/05